JC18 Rec'd PCT/PTO 10 JAN 2002

FORM PTO-1390 (Modified) (REV 11-2000) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371

ATTORNEY'S DOCKET NUMBER	U.S. APPLICATION NO. (IF KNOWN, SEE 37 CFR)
217883US3PCT	10/030435

INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/JP00/08105	16 November 2000	10 May 2000

TITLE OF INVENTION
METHOD OF MANUFACTURING MULTILAYER CIRCUIT BOARD

APPLICANT(S) FOR DO/EO/US
KARIYA Takashi

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. ☒ This is an express request to begin national examination procedures (35 U.S.C. 371(f)). The submission must include items (5), (6), (9) and (24) indicated below.
4. ☐ The US has been elected by the expiration of 19 months from the priority date (Article 31).
5. ☒ A copy of the International Application as filed (35 U.S.C. 371 (c) (2))
   a. ☐ is attached hereto (required only if not communicated by the International Bureau).
   b. ☒ has been communicated by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US).
6. ☒ An English language translation of the International Application as filed (35 U.S.C. 371(c)(2)).
   a. ☒ is attached hereto.
   b. ☐ has been previously submitted under 35 U.S.C. 154(d)(4).
7. ☒ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371 (c)(3))
   a. ☐ are attached hereto (required only if not communicated by the International Bureau).
   b. ☐ have been communicated by the International Bureau.
   c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   d. ☒ have not been made and will not be made.
8. ☐ An English language translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
9. ☒ An oath or declaration of the inventor(s) (35 U.S.C. 371 (c)(4)).
10. ☐ An English language translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371 (c)(5)).
11. ☐ A copy of the International Preliminary Examination Report (PCT/IPEA/409).
12. ☒ A copy of the International Search Report (PCT/ISA/210).

Items 13 to 20 below concern document(s) or information included:

13. ☒ An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
14. ☐ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
15. ☐ A **FIRST** preliminary amendment.
16. ☐ A **SECOND** or **SUBSEQUENT** preliminary amendment.
17. ☐ A substitute specification.
18. ☐ A change of power of attorney and/or address letter.
19. ☐ A computer-readable form of the sequence listing in accordance with PCT Rule 13ter.2 and 35 U.S.C. 1.821 - 1.825.
20. ☐ A second copy of the published international application under 35 U.S.C. 154(d)(4).
21. ☐ A second copy of the English language translation of the international application under 35 U.S.C. 154(d)(4).
22. ☐ Certificate of Mailing by Express Mail
23. ☒ Other items or information:

PCT/IB/304/Drawings (3 sheets)
Notice of Priority/Form PTO-1449

U.S. APPLICATION NO. (IF KNOWN, SEE 37 CFR)	INTERNATIONAL APPLICATION NO.	ATTORNEY'S DOCKET NUMBER
10/030435	PCT/JP00/08105	217883US3PCT

24. The following fees are submitted:.		CALCULATIONS PTO USE ONLY	
BASIC NATIONAL FEE (37 CFR 1.492 (a) (1) - (5)) :			
☐ Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO and International Search Report not prepared by the EPO or JPO	**$1040.00**		
☒ International preliminary examination fee (37 CFR 1.482) not paid to USPTO but International Search Report prepared by the EPO or JPO	**$890.00**		
☐ International preliminary examination fee (37 CFR 1.482) not paid to USPTO but international search fee (37 CFR 1.445(a)(2)) paid to USPTO	**$740.00**		
☐ International preliminary examination fee (37 CFR 1.482) paid to USPTO but all claims did not satisfy provisions of PCT Article 33(1)-(4)	**$710.00**		
☐ International preliminary examination fee (37 CFR 1.482) paid to USPTO and all claims satisfied provisions of PCT Article 33(1)-(4)	**$100.00**		
ENTER APPROPRIATE BASIC FEE AMOUNT =		**$890.00**	
Surcharge of **$130.00** for furnishing the oath or declaration later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492 (e)).		**$0.00**	

CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE		
Total claims	2 - 20 =	0	x $18.00	**$0.00**	
Independent claims	1 - 3 =	0	x $84.00	**$0.00**	
Multiple Dependent Claims **(check if applicable)**.			☐	**$0.00**	
TOTAL OF ABOVE CALCULATIONS =				**$890.00**	
☐ Applicant claims small entity status. See 37 CFR 1.27). The fees indicated above are reduced by 1/2.				**$0.00**	
SUBTOTAL =				**$890.00**	
Processing fee of **$130.00** for furnishing the English translation later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492 (f)). +				**$0.00**	
TOTAL NATIONAL FEE =				**$890.00**	
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31) **(check if applicable).** ☐				**$0.00**	
TOTAL FEES ENCLOSED =				**$890.00**	
				Amount to be: refunded	$
				charged	$

a. ☒ A check in the amount of **$890.00** to cover the above fees is enclosed.

b. ☐ Please charge my Deposit Account No. _____ in the amount of _____ to cover the above fees. A duplicate copy of this sheet is enclosed.

c. ☒ The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. **15-0030** A duplicate copy of this sheet is enclosed.

d. ☐ Fees are to be charged to a credit card. **WARNING:** Information on this form may become public. **Credit card information should not be included on this form.** Provide credit card information and authorization on PTO-2038.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO:

Surinder Sachar
Registration No. 34,423

22850

Surinder Sachar
SIGNATURE

C. Irvin McClelland
NAME

21,124
REGISTRATION NUMBER

Jan 10 2002
DATE

10/050477
JC13 Rec'd PCT/PTO 10 JAN 2002

3/prts

DESCRIPTION

METHOD OF MANUFACTURING MULTILAYER CIRCUIT BOARD

TECHNICAL FIELD

The present invention relates to a method of manufacturing a multilayer circuit board.

BACKGROUND ART

The build-up process is well known as a conventional method of manufacturing a multilayer circuit board. For example, a multilayer circuit board is manufactured as follows in this process. Firstly, via holes are formed at prescribed positions in a one-side copper-clad laminate manufactured by applying a copper foil to one side of an insulating substrate. The via holes are filled with an electrically conductive paste. A copper foil is bonded to the insulating substrate side of the one-side copper-clad laminate by pressing. The copper foil is etched so that a prescribed conductor circuit is formed.

A both printed board manufactured as described above serves as a core board. Insulating substrates are stacked on both sides of the core board respectively and bonded by pressing. Thereafter, via holes are formed at prescribed positions and then filled with the conductive paste. After copper foils are stacked on both sides of the board and pressed again, prescribed conductor circuits are formed on each copper foil. This step is repeated for further increase in the layers so that a multilayer circuit board is manufactured.

In the foregoing method, the both printed board serving as the core board is manufactured and circuit patterns are sequentially stacked on the core board. Accordingly, since the number of steps is increased, there is a definite limit in improvement of the manufacturing efficiency.

Furthermore, manufacture of the core board requires a step of bonding a copper foil by pressing in the conventional method. The pressing sometimes distorts the insulating substrate of the core board, whereupon positions of the via holes formed in the insulating substrate are sometimes displaced. Accordingly, a land needs to be rendered larger in consideration of allowance for displacement. This results in a problem that densification of the multilayer circuit board is difficult.

Additionally, when the insulating substrates are stacked on the core board, the pressing sometimes causes misregistration between the core substrate and each insulating board. Accordingly, an X-ray check hole needs to be previously formed so that the location of the inner conductor circuit is checked from the surface of the insulating board. This necessitates one extra step in the manufacture.

DISCLOSURE OF THE INVENTION

A first invention is a method of manufacturing a multilayer circuit board, in which a plurality printed board are stacked and pressed into a multilayer circuit board, each printed board having a conductor layer on one side of an insulating layer, characterized by the steps of stacking the printed boards with a bonding layer being interposed between the printed boards, and

stacking an outermost conductor layer on an insulating layer side of a first outermost printed board with a bonding layer being interposed therebetween and pressing a stack so that the printed boards and the outermost conductor layer are bonded together, the first outermost printed board being disposed with the insulating layer side being directed outward.

A second invention is characterized in that the printed boards include a second outermost printed board disposed with a conductor layer side being directed outward, the conductor layer being pressed under a condition where the conductor layer has a uniform thickness all over.

According to the first invention, the printed boards each of which has one side formed with a conductor layer are stacked. The outermost conductor layer is stacked on the insulating layer side of the first outermost printed board disposed with the insulating layer side being directed outward. The printed boards are collectively pressed to be manufactured into a multilayer circuit board. Accordingly, the multilayer circuit board is manufactured by a single pressing operation. Consequently, the manufacturing steps can be simplified and the manufacturing efficiency can be improved.

Furthermore, since pressing is carried out just once, the possibility that the insulating substrate may be distorted and the possibility that the printed board may be shifted can be rendered minimum. Consequently, the precision of the multilayer circuit board can be improved.

According to the second invention, the second outermost printed board is not previously etched and pressed under the

condition where the thickness thereof is entirely uniform. Accordingly, since a uniform pressure is applied to the whole printed board in the pressing, the possibility of distortion and displacement can be rendered minimum. Consequently, the precision of the multilayer circuit board can be improved.

BIREF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a sectional view (1) showing steps of manufacturing a multilayer circuit board of one embodiment in accordance with the present invention;

FIG. 2 is a sectional view (2) showing steps of manufacturing a multilayer circuit board of the embodiment in accordance with the present invention; and

FIG. 3 is a sectional view (3) showing steps of manufacturing a multilayer circuit board of the embodiment in accordance with the present invention.

BEST MODE FOR ENFORCEMENT OF THE INVENTION

One embodiment of the present invention will be described with reference to FIGS. 1 to 3.

In the method of manufacturing the multilayer circuit board 1 in accordance with the present invention, a plurality printed board 2 are stacked and collectively pressed. The method is characterized by stacking an outermost copper foil 6 (corresponding to an outermost conductor layer of the present invention) on a side of a first outermost printed board 2A at an insulating substrate 4A side and pressing, the printed board 2A having an insulating substrate 4 (corresponding to an

insulating layer in the present invention) side being directed outward. See FIG. 2(G).

The method is further characterized in that a copper foil 5B of a second outermost printed board 2B disposed with the copper foil 5B (corresponding to a conductor layer in the present invention) side being directed outward is not previously formed with a conductor circuit 10 and is pressed under a condition where the copper foil 5B remains on the whole side.

The manufacture of the printed board 2 forming the multilayer circuit board 1 starts with a one-side copper-clad laminate 3. The one-side copper-clad laminate 3 has a well known structure, that is, the copper foil 5 is affixed to overall one side of an insulating substrate 4 (the underside in FIG. 1) made of a plate-shaped glass-cloth epoxy resin (FIG. 1(A)).

Laser beams are irradiated onto prescribed locations on the insulating substrate 4 from the side of the substrate opposite the copper foil 5 (the upper side in FIG. 1) so that via holes 7 extending through the insulating substrate to the copper foil 5 are formed (FIG. 1(B)). The laser beam machining is executed by a pulse oscillation CO_2 gas laser, for example. In this case, the pulse energy preferably ranges between 2.0 and 10.0 mJ, the pulse width preferably ranges between 1 and 100 μs, the pulse interval is preferably at or above 0.5 ms, and the number of shots preferably ranges between 3 and 50.

Thereafter, desmearing is carried out in order that resin remaining in the via holes 7 may be removed. The desmearing includes a treatment of potassium permanganate, oxygen plasma discharge, corona discharge process, etc.

Subsequently, the copper foil 5 is covered with a protecting film made from polyethylene terephthalate although this state is not shown. In this state, a plated conductor 8 is formed in each via hole 7 by an electroplating with the copper foil 5 serving as one of electrodes (FIG. 1(C)). An amount of conductor 8 filling each via hole 7 is preferably determined so that an upper face thereof is slightly lower than the surface of the insulating substrate 4. Copper is most preferably as a plated metal but may be any metal which can be plated, such as tin, silver, solder, alloy of copper and tin, alloy of copper and silver, etc.

An electrically conductive bump 9 comprising a material with a low melting point, such as tin is formed by means of bump plating so that the bump overlaps the plated conductor 8 in each via hole 7. Each conductive bump 9 is formed so as to project slightly from the upper surface of the insulating substrate 4 (FIG. 1(D)). Subsequently, the copper foil 5 is etched so that a conductor circuit 10 is formed after the protecting film is stripped from the copper foil 5 (FIG. 1(E)).

A thermosetting adhesive (epoxy resin adhesive, for example) is applied by roll coating to the side of the printed board 2 on which the conductive bumps 9 are formed, whereby an adhesive layer 11 is formed (FIG. 1(F)).

A plurality of printed boards 2 manufactured as described above are aligned and overlapped (FIG. 2G). A second outermost printed board 2B of the top layer is overlapped without being etched. Accordingly, the copper foil 5 remains on the printed board 2B with a uniform thickness over the whole surface. The printed board 2B is disposed so that the copper foil 5 is directed

outward (upward in FIG. 2) and the conductive bumps 9 are directed inward. The printed board 2 located below the printed board 2B is stacked so that the conductor circuits 10 are positioned at the upper side of the printed board 2. Thus, the printed boards are stacked so that the conductive bumps 9 of the printed board 2 located upward are connectable to the conductor circuits 10 of the lower printed board 2. Additionally, a first outermost printed board 2A located lowermost is stacked so that the insulating substrate 4A side formed with the adhesive layer is directed outward (downward in FIG. 2). An outermost copper foil 6 is stacked on the surface of the printed board 2A.

The printed boards thus stacked are heated and pressed under vacuum at 180°C for 70 minutes so that the adhesive layer 11 is hardened, whereby the printed boards 2, 2A and 2B, and the outermost copper foil 6 are bonded together. The multilayer circuit board 11 in which the printed boards 2, 2A and 2B and outermost copper foil 6 are integrated is manufactured by one pressing operation (FIG. 2(H)). The distal ends of the conductive bumps 9 of each printed board are connected to prescribed locations of the conductor circuit 10 on the adjacent printed board 2, whereupon the conductor circuits 10 of the adjacent printed boards 2 are electrically connected to each other.

Subsequently, the copper foil 5 on the uppermost side and the outermost copper foil 6 affixed to the underside are etched so that conductor circuits 10 are formed (FIG. 3(I)).

A photosensitive solder resist 12 is applied to the whole underside and exposure and development processes are applied to the solder resist in a prescribed pattern so that the solder resist

12 is formed with openings which open lands formed at prescribed locations on the conductor circuit 10. Pins 13 for connecting the multilayer circuit board 1 to other components are bonded to the lands by solder 14. The multilayer circuit board 1 is thus manufactured.

According to the foregoing embodiment, the multilayer circuit board 1 is manufactured by stacking a plurality of printed boards 2 and stacking the outermost copper foil 6 on the insulating substrate 4A side of the first outermost printed board 2A disposed with the insulating substrate side being directed outward, and collectively pressing the stack. Accordingly, the multilayer circuit board 1 can be manufactured by a single time of pressing. Consequently, manufacturing steps can be simplified and the precision of the multilayer circuit board can be improved.

Furthermore, since pressing is carried out just once, the possibility that the insulating substrate 4 and the via holes 7 may be displaced can be rendered minimum. Consequently, the precision of the multilayer circuit board can be improved.

Furthermore, the copper foil 5B of the second outermost printed board 2B disposed with the copper foil side being directed outward is not previously etched, and the printed board 2B is pressed under the condition where the copper foil 5B having a uniform thickness all over is present. Accordingly, a uniform pressure can be applied to the whole printed board 2 and accordingly, the possibility that inner printed board 2 may be shifted or distorted can be rendered minimum. Consequently, the precision of the multilayer circuit board 1 can be improved.

The method of manufacturing the multilayer circuit board

1 can be applied to the manufacture of packages required of a particularly high precision. The underside on which the pins 13 are provided is preferably the outermost copper foil 6 side. The precision required for the lower layer side is lower than the precision required for the upper layer side and accordingly, the precision does not result in a problem even if the outermost copper foil 6 is stacked on the lowermost layer and pressed.

The technical scope of the present invention should not be limited by the above-described embodiment and covers equivalents thereof.

INDUSTRIAL APPLICABILITY

The present invention can provided a method of manufacturing a multilayer circuit board which can simplify the manufacturing steps and improve the precision of the multilayer circuit board.

CLAIMS

1. A method of manufacturing a multilayer circuit board, in which a plurality printed board are stacked and pressed into a multilayer circuit board, each printed board having a conductor layer on one side of an insulating layer, characterized by the steps of stacking the printed boards with a bonding layer being interposed between the printed boards, and stacking an outermost conductor layer on an insulating layer side of a first outermost printed board with a bonding layer being interposed therebetween and pressing a stack so that the printed boards and the outermost conductor layer are bonded together, the first outermost printed board being disposed with the insulating layer side being directed outward.

2. A method of manufacturing according to claim 1, characterized in that the printed boards include a second outermost printed board disposed with a conductor layer side being directed outward, the conductor layer being pressed under a condition where the conductor layer has a uniform thickness all over.

OBLON ET AL. (703) 413-3000
DOCKET # AI7883053PCT SHEET 1 OF 3

FIG. 1

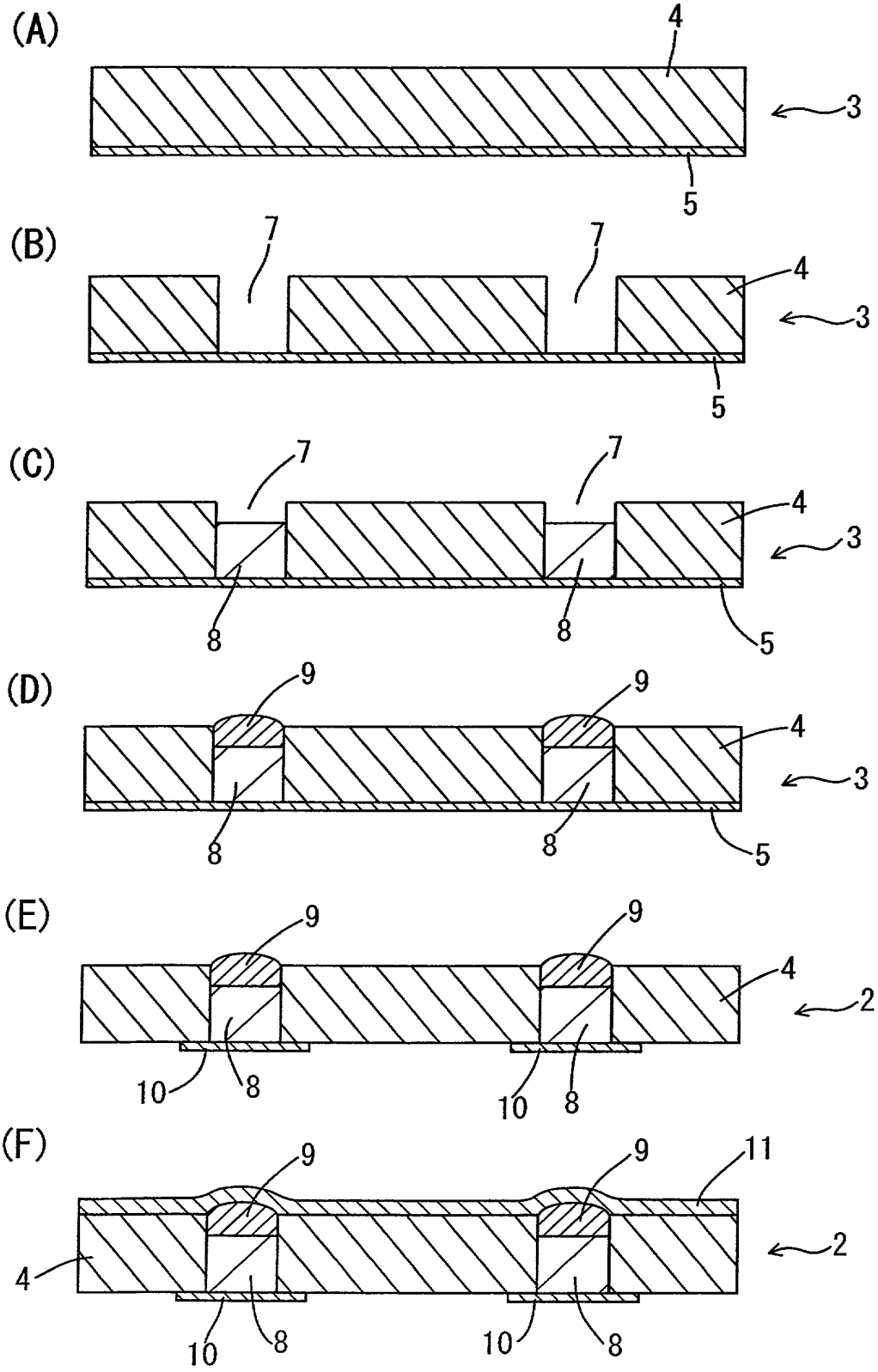


FIG. 2

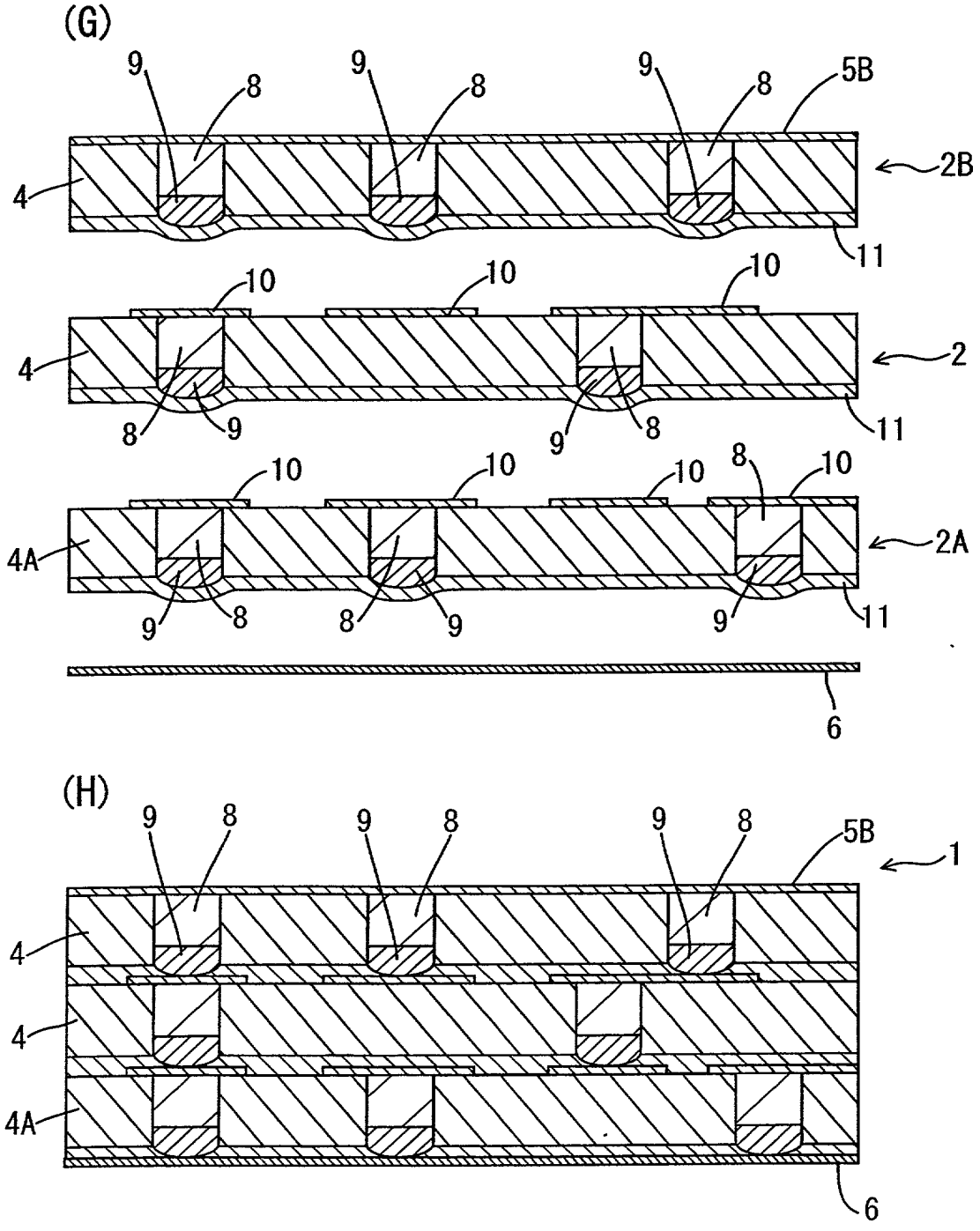
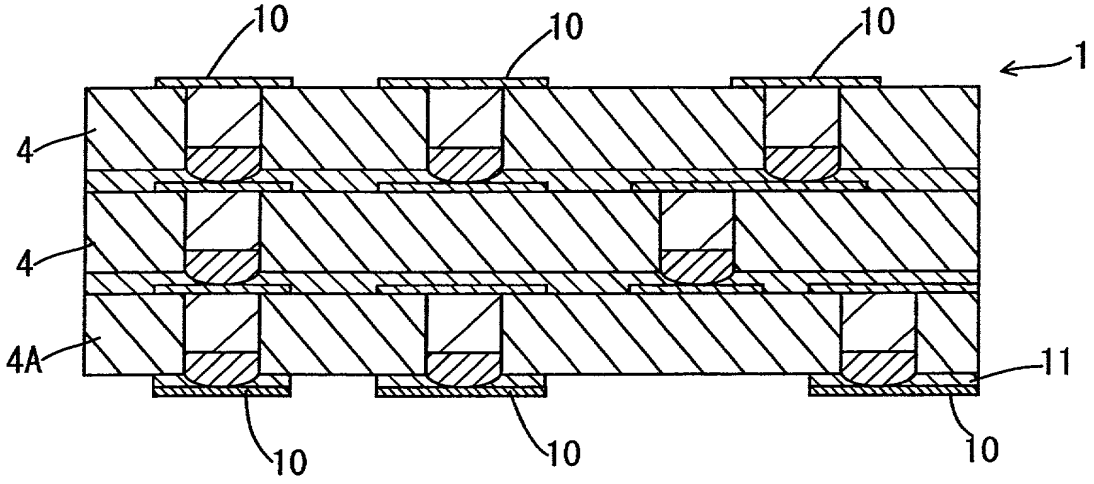


FIG. 3

(I)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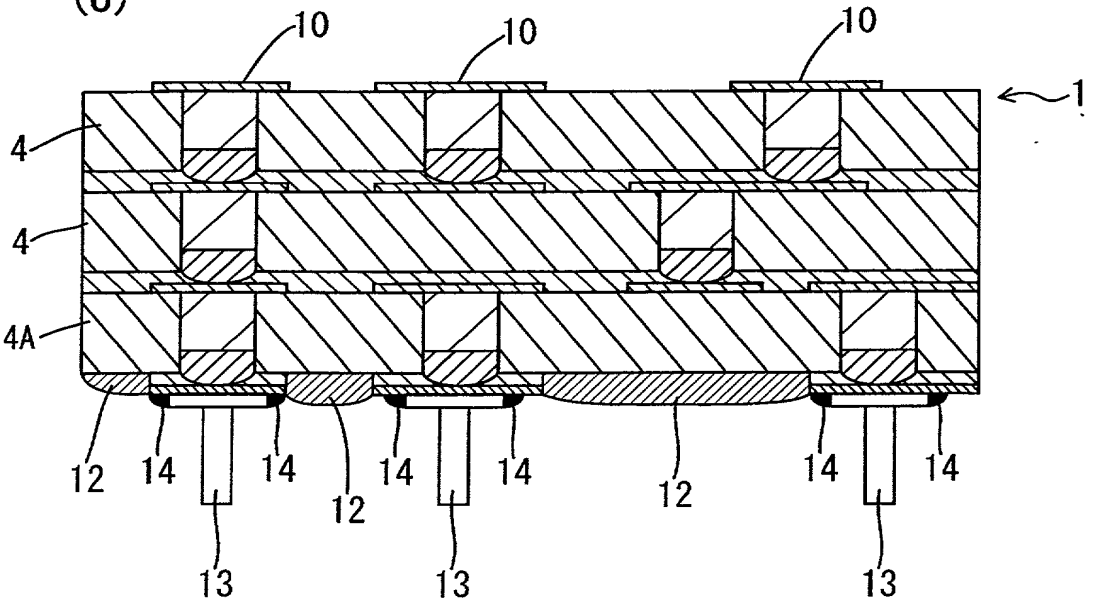
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Declaration and Power of Attorney For Patent Application

特許出願宣言書及び委任状

Japanese Language Declaration

日本語宣言書

下記の氏名の発明者として、私は以下の通り宣言します。

As a below named inventor, I hereby declare that:

私の住所、私書箱、国籍は下記の私の氏名の後に記載された通りです。

My residence, post office address and citizenship are as stated next to my name.

下記の名称の発明に関して請求範囲に記載され、特許出願している発明内容について、私が最初かつ唯一の発明者（下記の氏名が一つの場合）もしくは最初かつ共同発明者（下記の名称が複数の場合）であると信じています。

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled.

METHOD OF MANUFACTURING MULTILAYER CIRCUIT BOARD

上記発明の明細書は、

- ☐ 本書に添付されています。
- ☐ ___月___日に提出され、米国出願番号または特許協定条約国際出願番号を_____とし、
  （該当する場合）_____に訂正されました。

the specification of which

- ☐ is attached hereto.
- ☒ was filed on November 16, 2000
  as ~~United States Application Number or~~ XXXXXXXXXXXXXXXXXXXXXXXXXX
  PCT International Application Number
  PCT/JP00/08105 and was amended on
  _____ (if applicable).

私は、特許請求範囲を含む上記訂正後の明細書を検討し、内容を理解していることをここに表明します。

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

私は、連邦規則法典第37編第1条56項に定義されるとおり、特許資格の有無について重要な情報を開示する義務があることを認めます。

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

Japanese Language Declaration
(日本語宣言書)

私は、米国法典第35編119条（a）-（d）項又は365条（b）項に基づき下記の、米国以外の国の少なくとも一ヵ国を指定している特許協力条約365（a）項に基づく国際出願、又は外国での特許出願もしくは発明者証の出願についての外国優先権をここに主張するとともに、優先権を主張している、本出願の前に出願された特許または発明者証の外国出願を以下に、枠内をマークすることで、示しています。

I hereby claim foreign priority under Title 35, United States Code, Section 119 (a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or Section 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)
外国での先行出願

(Number) (番号)	(Country) (国名)	(Day/Month/Year Filed) (出願年月日)	Priority Claimed 優先権主張 Yes はい	No いいえ
2000-137144	Japan	May 10, 2000	☒	☐
			☐	☐

私は、第35編米国法典119条（e）項に基づいて下記の米国特許出願規定に記載された権利をここに主張いたします。

I hereby claim the benefit under Title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below.

(Application No.) (出願番号)	(Filing Date) (出願日)

私は、下記の米国法典第35編120条に基づいて下記の米国特許出願に記載された権利、又は米国を指定している特許協力条約365条（c）に基づく権利をここに主張します。また、本出願の各請求範囲の内容が米国法典第35編112条第1項又は特許協力条約で規定された方法で先行する米国特許出願に開示されていない限り、その先行米国出願書提出日以降で本出願書の日本国内または特許協力条約国際提出日までの期間中に入手された、連邦規則法典第37編1条56項で定義された特許資格の有無に関する重要な情報について開示義務があることを認識しています。

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s), or Section 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of Title 35, United States Code Section 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of application.

(Application No.) (出願番号)	(Filing Date) (出願日)	(Status: Patented, Pending, Abandoned) (現況：特許許可済、係属中、放棄済)

私は、私自信の知識に基づいて本宣言書中で私が行なう表明が真実であり、かつ私の入手した情報と私の信じるところに基づく表明が全て真実であると信じていること、さらに故意になされた虚偽の表明及びそれと同等の行為は米国法典第18編第1001条に基づき、罰金または拘禁、もしくはその両方により処罰されること、そしてそのような故意による虚偽の声明を行なえば、出願した、又は既に許可された特許の有効性が失われることを認識し、よってここに上記のごとく宣誓を致します。

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Japanese Language Declaration
(日本語宣言書)

委任状：私は下記の発明者として、本出願に関する一切の手続きを米特許商標局に対して遂行する弁理士または代理人として、下記の者を指名いたします。
(弁護士、または代理人の指名及び登録番号を明記のこと)

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith: *(list name and registration number)*

022850

書類送付先

Send Correspondence to:

022850

直接電話連絡先：（名前及び電話番号）

Direct Telephone Calls to: (name and telephone number)

(703) 413-3000

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第二の共同発明者の氏名	Full name of second joint inventor, if any
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(第三以降の共同発明者についても同様に記載し、署名すること)

(Supply similar information and signature for third and subsequent joint inventors.)